

CLOCK GENERATOR FOR GENERATING ACCURATE
AND LOW-JITTER CLOCK

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ABSTRACT OF THE DISCLOSURE

A clock generator has a clock generating circuit, a phase difference detection circuit, and a control signal generating circuit. The clock generating circuit has a function for varying a clock phase in accordance with a control signal, the phase difference detection circuit compares the clock phase output from the clock generating circuit with a phase of a reference waveform, and detecting a phase difference therebetween, and the control signal generating circuit generates a control signal for controlling the clock phase of the clock generating circuit, based on phase difference information obtained from the phase difference detection circuit. The phase difference detection circuit has a plurality of phase detection units, at least one of the plurality of phase detection units carries out a direct phase detection in which a phase of the clock is directly compared with the phase of the reference waveform, and at least the other one of the plurality of phase detection units carries out an indirect phase detection using a phase-synchronized waveform generating circuit generating a waveform synchronized in phase with the reference waveform or an output of the clock generating circuit and a phase information extracting circuit extracting phase information from the phase-synchronized waveform.